IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A method of vertically stacking wafers, comprising:

selectively depositing a plurality of metallic lines on opposing surfaces of each of a first wafer and a second wafer ~~adjacent wafers~~;

bonding the first wafer to the second wafer by bonding the ~~adjacent wafers, via~~ respective metallic lines on opposing surfaces of the first wafer and the second wafer ~~adjacent wafers~~ to create a vertically stacked wafer pair; ~~to establish electrical connections between active devices on vertically stacked wafers, and~~

forming one or more vias to establish electrical connections between the active devices on each wafer of ~~on~~ the vertically stacked wafer pair ~~wafers~~ and an external interconnect, the vias tapered from top to bottom hole, such that a top surface of each via has a larger area than a bottom surface; and

bonding two vertically stacked wafer pairs together by bonding the top surfaces of each of the one or more vias of a first vertically stacked wafer pair to corresponding top surfaces of each of the one or more vias of a second vertically stacked wafer pair.

2. (Currently Amended) The method as claimed in claim 1, wherein each via is formed by:

selectively etching the top wafer to form a via;

depositing an oxide layer to insulate a sidewall of the via;

forming a barrier/seed layer in the via;

depositing a barrier layer in the via;

depositing a seed layer on the barrier layer; and

depositing a conduction metal on the ~~barrier/~~seed layer in the via for providing an electrical connection between active devices on the vertically stacked wafers and the external interconnect.

3. (Original) The method as claimed in claim 1, wherein the metallic lines are Copper (Cu) lines deposited to serve as electrical contacts between active devices on the vertically stacked wafers.

4. (Original) The method as claimed in claim 2, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy.

5. (Cancelled)

6. (Currently Amended) The method as claimed in claim ~~5~~ 2, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

7. (Currently Amended) The method as claimed in claim 1, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures ~~such as ground planes or heat conduits~~ for the active devices on the vertically stacked wafers.

8. (Cancelled)

9. (Currently Amended) The method as claimed in claim 1, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of a via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

selectively etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;

depositing a barrier layer in the via;

depositing a seed layer on the barrier layer; and

~~depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and~~

depositing a conduction metal on the ~~barrier~~/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and an external interconnect.

10. (Currently Amended) The method as claimed in claim 9, wherein the ~~barrier/seed layer includes a~~ barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and ~~a~~ the

copper (Cu) seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer, ~~and~~ deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

11. (Original) The method as claimed in claim 1, wherein the vias are formed during a Shallow Trench Isolation (IST) process in the top wafer before the adjacent wafers are bonded, via the respective metallic lines deposited on opposing surfaces of the adjacent wafers.

12 – 32. (Cancelled)